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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/801,812	02/14/97	GIVENS J	11675.106

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BRADLEY K DESANDRO
WORKMAN NYDEGGER AND SEELEY
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY UT 84111

EXAMINER
EATON,K

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/26/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/801,812	Applicant(s) Givens
	Examiner Kurt Eaton	Group Art Unit 2814

☒ Responsive to communication(s) filed on *Apr 7, 1999* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-28* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-28* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Feb 14, 1997* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I (claims 1-28) in Paper No. 4 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the step of removing (by an abrasive planarization/ CMP step) portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material must be shown or the feature(s) cancelled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29-35 have been canceled.

5. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madokoro in view of Fiordalice et al. '072.

Madokoro shows, in an analogous art related to a method for forming an Al layer by the use of a laser flow technique, in Figures 1(a) and 1(b) forming a recess, by patterning and etching, a dielectric material (15) situated on a semiconductor lower substrate (11), the recess extending below a top surface of the dielectric material; forming a barrier layer (17), made of TaSi, on the recess within the dielectric material; forming an electrically conductive layer (18), made out of material including of aluminum, on the barrier layer, the material from which the barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed; forming an energy absorbing layer (19), made out of material selected from the group including W, TiW, TiN, etc., on the electrically conductive layer, the energy absorbing layer having a greater light absorption capacity than that of the electrically conductive layer; applying energy, by utilizing a laser as an energy source, to the energy absorbing layer so as to heat the electrically conductive layer and to cause the electrically conductive layer to flow within the recess; and removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material by patterning and etching, thereby creating interconnects {column 3, lines 12-39; column 4, line 46 - column 5, line 39}.

It would have been inherent to one of ordinary skill in the art at the time the invention was made that since the energy absorbing layer of Madokoro had a higher light absorption capacity

than the electrically conductive layer, the energy absorbing layer would thus also have a higher heat absorption capacity than the electrically conductive layer.

Madokoro does not show forming the barrier layer such that it includes two separate layers including a metallic diffusion barrier layer made of CVD TiN and a metallic seed layer on the diffusion barrier layer made of CVD TiN; and wherein, prior to the step of forming the seed layer on the diffusion barrier layer, the diffusion barrier layer is heated in an environment substantially containing a nitrogen gas.

Fiordalice et al. '072 (herein referred to as Fiordalice 072) shows, in an analogous art related to a method for forming a conductive interconnect in an integrated circuit, in Figures 1-8 forming a recess within a dielectric material (14) situated on a semiconductor lower substrate (12), the recess extending below a top surface of the dielectric material; forming a metallic diffusion barrier (22) made of CVD TiN on the recess within the dielectric material; forming a metallic seed layer (24) made of CVD TiN on the diffusion barrier wherein, prior to the step of forming the seed layer on the diffusion barrier layer, heating the diffusion barrier layer in an environment substantially containing nitrogen gas; forming an electrically conductive layer made of aluminum material; and forming an interconnect by either patterning and etching the material above the top surface of the dielectric material or planarizing the material above the top surface of the dielectric layer {column 2, line 56 - column 3, line 43; column 4, line 18 - column 5, line 4}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the barrier layer of Madokoro using the method and materials of Fiordalice 072 to

form a barrier layer that composed a CVD TiN diffusion barrier layer and a CVD TiN seed layer since the equivalence of a TiN bi-layer and a TaSi barrier layer for their use in interconnect barrier metallization and the selection of either of these known equivalents to prevent aluminum spiking into the substrate region of a semiconductor device would be within the level of ordinary skill in the art.

6. Claims 12, 13, 15-20, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madokoro in view of Fiordalice 072 as applied to claim 1 above, and further in view of Fiordalice et al. '523.

Madokoro in view of Fiordalice 072 substantially discloses the method as claimed but fails to show wherein the step of removing portions of the energy absorbing layer and the electrically conductive layer is an abrasive, chemical mechanical, planarization step or wherein the recess includes a contact hole situated below a trench, the semiconductor substrate assembly having a lower substrate defining a plane, the contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at the trench, the trench extending from the opposite end of the contact hole to a top surface of the dielectric material, the trench extending substantially parallel to the plane of the lower substrate.

Fiordalice et al. '523 (herein referred to as Fiordalice 523) shows, in an analogous art related to methods for forming inlaid interconnects and polishing interconnect metal layers, in Figures 5-7 forming a recess (32) within a dielectric material wherein the recess includes a contact hole (34) situated below a trench (36), the semiconductor substrate assembly having a lower

substrate (26) defining a plane, the contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at the trench, the trench extending from the opposite end of the contact hole to a top surface of the dielectric material; forming electrically conductive Al material (42) in the contact hole and over the top surface of the dielectric layer (30); forming TiN material (31) over the top surface of the dielectric material; and removing portions of the TiN material and the Al material above the top surface of the dielectric material by a CMP step {column 5, line 33 - column 6, line 9; column 7, lines 3-17; column 8, lines 15-21}.

It would have been inherent to one of ordinary skill in the art at the time the invention was made that the trench of Fiordalice 523 would have extended substantially parallel to the plane of the lower substrate since, as shown in the above referenced Figures, there is no indication of any sort that the trench would not extend substantially parallel to the plane of the lower substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recess of Madokoro in view of Fiordalice 072 such that it had a contact hole situated below a trench wherein the semiconductor substrate assembly having a lower substrate defining a plane, the contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at the trench, the trench extending from the opposite end of the contact hole to a top surface of the dielectric material as in Fiordalice 523 since this recess configuration would have been an obvious design choice. It also would have been obvious to remove the electrically conducive layer and the energy absorbing layer of Madokoro in view of Fiordalice 072 using a CMP step as shown in Fiordalice 523 since equivalence of removing unwanted material above a

top surface of a dielectric layer by CMP and by patterning and etching for their use in creating interconnects and the selection of any of these known equivalents to aid in the formation of interconnect structures would be within the level of ordinary skill in the art.

7. Claims 14 and claims 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madokoro in view of Fiordalice 072 as applied to claim 1 above, and over Madokoro in view of Fiordalice 072 and Fiordalice 523 as applied to claim 16 above, respectively, and further in view of Kataoka et al..

The inventions of Madokoro in view of its modifiers substantially discloses the method as claimed but fails to show wherein the recess has an aspect ratio greater than about 4:1.

Kataoka et al. (herein referred to as Kataoka) shows, in an analogous art related to a process for forming metal films, materials such as aluminum and titanium may be deposited into recesses with aspect ratios greater than 1 {column 6, line 20 - column 8, line 4}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recess in the inventions of Madokoro in view of its modifiers such that it had an aspect ratio greater than about 4:1 as in Kataoka since discovering the optimum or workable ranges involves only routine skill in the art.

8. Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madokoro in view of Fiordalice 072 and Fiordalice 523 as applied to claim 16 above, and further in view of Sirkin.

The invention of Madokoro in view of its modifiers substantially discloses the method as claimed but fails to show wherein the dielectric material is formed on a monocrystalline silicon layer of semiconductor substrate assembly, wherein the monocrystalline silicon layer defines a plane.

Sirkin shows, in an analogous art related to a contact structure using a barrier metal and a method of making the same, in Figure 1A forming a dielectric layer (12) on a monocrystalline silicon layer (10) of a semiconductor substrate assembly wherein the monocrystalline silicon layer defines a plane {column 2, lines 43-48}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor lower substrate of Madokoro in view of its modifiers out of monocrystalline silicon since, within the general skill of a worker in the art, to select a known material on the basis of its suitability for its intended use is a matter of obvious design choice.

Conclusion

9. Paper related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in the Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722 or -7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by E-mail via **Kurt.Eaton@uspto.gov**.

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800